SOFTWARE-TO-HARDWARE COMPILER

Abstract of the Disclosure

A software-to-hardware compiler is provided that generates hardware constructs in programmable logic based on pure software constructs. More particularly, a high-level program language may be used to create a program using only software constructs that is compiled into hardware constructs. Optimizations may be made in the later stages of compilation to retime the circuit, allowing for maximum data flow. The hardware may make run-time decisions with respect to executing programmable logic blocks in parallel. The decisions may be at least partially based on a control flow.